What is Claimed is:

1. A digital system comprising:

at least a first processor;

a local memory connected to the first processor, the local memory operable to respond to transfer requests from the first processor, the local memory comprising a data array arranged as a plurality of segments and a plurality of indicator bits, wherein each of the plurality of segments has a corresponding indicator bit within the plurality of indicator bits; and

direct memory access (DMA) circuitry connected to the local memory, the DMA circuitry operable to transfer data to a selectable portion of segments of the plurality of segments from a selectable region of a second memory and operable to manipulate a selected portion of indicator bits of the plurality of indicator bits corresponding to the selectable portion of segments.

2. The digital system of Claim 1, wherein the plurality of indicator bits are valid bits operable to indicate that a corresponding segment contains valid data; and

wherein the DMA circuitry is operable to set to a valid state the selected portion of indicator bits corresponding to the selectable portion of segments.

3. The digital system of Claim 2, further comprising miss detection circuitry connected to the plurality of valid bits, the miss detection circuitry having a miss signal for indicating when a miss is detected in response to a request from the first processor to a first segment; and

wherein the processor stalls in response to the miss signal until the DMA circuitry sets a first valid bit corresponding to the first segment to a valid state.

4. The digital system of Claim 3, further comprising timeout circuitry connected in a responsive manner to the miss signal having an output connected to an interrupt input of the first processor, whereby the timeout circuit is operable to interrupt the processor if the DMA circuitry does not validate the first segment within a certain period of time.

5. The digital system of Claim 2, further comprising:

miss detection circuitry connected to the plurality of valid bits, the miss detection circuitry having a miss signal for indicating when a miss is detected in response to a request from the first processor to a first segment; and

address circuitry responsively connected to the miss signal, the address circuitry operable to transfer data to the first segment in response to the miss signal.

6. The digital system of Claim 5, wherein the DMA circuitry is operable to transfer a block of data to the selected portion of segments in such a manner that a transfer to the first segment holding valid data within the selected portion of segments is inhibited.

7. The digital system of Claim 1, wherein the plurality of indicator bits are dirty bits operable to indicate that a corresponding segment contains dirty data.

8. The digital system of Claim 7, wherein the DMA circuitry is operable to transfer data from a selectable portion of segments to a selectable region of the second memory in accordance with a corresponding portion of dirty bits, such that only segments within the selectable portion of segments whose corresponding dirty bit is in a dirty state are transferred.

9. The digital system of Claim 8, wherein a first dirty bit is operable to be set to a dirty state in response to a write transaction by the first processor to a first segment associated with the first dirty bit, and

wherein the first dirty bit is operable to be set to a dirty state in response to a write transaction by the DMA circuitry to the first segment associated with the first dirty bit.

10. The digital system of Claim 9, further comprising a first mode circuit connected to DMA circuitry, wherein the DMA circuitry is operable to transfer a block of segments from the local memory to the second memory in a manner that only segments within the block marked as dirty are transferred when the first mode circuit is in a first state, and wherein the DMA circuitry is operable ignore the plurality of dirty bits such that the entire block is transferred when the first mode circuit is in a second state.

11. The digital system according to Claim 1 being a cellular telephone, further comprising:

an integrated keyboard connected to the CPU via a keyboard adapter;

a display, connected to the CPU via a display adapter;

radio frequency (RF) circuitry connected to the CPU; and

an aerial connected to the RF circuitry.

12. A method of operating a digital system having a processor and a local memory, comprising the steps of:

organizing the local memory as a plurality of segments;

associating a plurality of indicator bits with the plurality of segments such that each segment has at least one corresponding indicator bit; and

setting a first indicator bit associated with a first segment in the local memory to a first state in response to a direct memory access (DMA) transfer of a

first data value from a selectable location in a second memory to the first location in the local memory.